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Customer No.: 31561
Application No.: 10/604,042
Docket No.: 9265-US-PA

Amendments

In the Specification

[0009] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a three-dimensional memory structure. The memory structure comprises a multiple of stacked circuits. The first stacked circuit includes two ~~conductive layers, an~~ n-type polysilicon layers, a ~~p-type polysilicon~~ conductive layer and an anti-fuse. ~~The n-type polysilicon layer in the first stacked circuit is located between the two conductive layers and the p-type polysilicon layer is located between the n-type polysilicon layer and one of the two conductive layers.~~ The anti-fuse and the conductive layer ~~is~~ are located between the n-type polysilicon layers ~~and the other one of the two conductive layers~~. Hence, the first stacked circuit includes ~~a conductive layer/p-type polysilicon layer/n-type polysilicon layer/anti-fuse/conductive layer (C/P/N/A/C)~~ an n-type polysilicon layer/anti-fuse/conductive layer/n-type polysilicon layer (N/A/C/N) setup and ~~a conductive layer/anti-fuse/n-type polysilicon layer/p-type polysilicon layer/conductive layer (C/A/N/P/C)~~ an n-type polysilicon layer/ conductive layer /anti-fuse /n-type polysilicon layer (N/C/A/N) setup.

[0010] The second stacked circuit of the three-dimensional memory structure includes two ~~conductive layers, an n-type polysilicon layer, a~~ p-type polysilicon layers, a conductive

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layer and an anti-fuse. ~~The p-type polysilicon layer of the second stacked circuit is located between the two conductive layers and the n-type polysilicon layer is located between the p-type polysilicon layer and one of the conductive layers.~~ The anti-fuse and the conductive layer are ~~is~~ located between the p-type polysilicon ~~and the other one of the two conductive~~ layers. Hence, the second stacked circuit includes a ~~conductive layer/anti-fuse/p-type polysilicon layer/n-type polysilicon layer/conductive layer (C/A/P/N/C)~~ p-type polysilicon layer/ conductive layer/anti-fuse /p-type polysilicon layer (P/C/A/P) setup and a ~~conductive layer/n-type polysilicon layer/~~p-type polysilicon layer/anti-fuse/conductive layer/p-type polysilicon layer (P/A/C/P) ~~(C/N/P/A/C)~~ setup. The second stacked circuit and the first stacked circuit cross over and perpendicular to each other ~~in the vertical dimension~~. Therefore, a total of four different methods of combining the first stacked circuit and the second stacked circuit are possible. In addition, according to the memory capacity, one of the four aforementioned configurations can be used to form more stacked circuits over the substrate.

Please amend paragraph [0011] of the specification as follow:

[0011] This invention also provides a method of fabricating a three-dimensional memory structure. First, an n-type polysilicon layer/conductive layer/anti-fuse/n-type polysilicon layer (N/C/A/N) stack structure is formed over a substrate. The N/C/A/N stack structure is patterned to form an array of linear first stacked lines. Thereafter, a dielectric layer is

formed in the space between the first stacked lines above the substrate. The dielectric layer is planarized to expose the topmost n-type polysilicon layer of the first stacked lines. A p-type polysilicon/conductive layer/anti-fuse/p-type polysilicon layer (P/C/A/P) stacked structure is formed over the topmost n-type polysilicon layer of the first stacked line. Next, the P/C/A/P stacked structure and the topmost n-type polysilicon layer of the first stacked line is patterned to form an array of linear second stacked lines that crosses over and perpendicular to the first stacked lines ~~vertically~~. Another dielectric layer is formed in the space between the second stacked lines above the anti-fuse of the first stacked lines. The dielectric layer is again planarized to expose the topmost p-type polysilicon layer of the second stacked lines. The overlapping areas between the first stacked lines and the second stacked lines forms an array of cylindrical memory cells. The aforementioned processing steps are repeated to form more stacked lines and hence build up a three-dimensional memory structure.

Please amend paragraph [0017] of the specification as follow:

[0017] Figs. 2A and 2B are front views and side view of a three-dimensional memory structure according to one preferred embodiment of this invention. As shown in Figs. 2A and 2B, the three-dimensional structure comprises of a stack of circuit layers. The first stack circuit 21 includes two n-type polysilicon layers 23 and 25, a conductive layer 27 and an anti-fuse 29. The anti-fuse 29 is a silicon oxide layer and the conductive layer 27 is a

tungsten silicide or a titanium silicide layer, for example. The conductive layer 27 of the first stack circuit 21 is located between the two n-type polysilicon layers 23 and 25. The anti-fuse 29 is located between the n-type polysilicon layer 25 and the conductive layer 27. Hence, the first stack circuit 21 has an n-type polysilicon/conductive layer/anti-fuse/n-type polysilicon (N/C/A/N) setup. The second stack circuit 31 of the three-dimensional memory structure includes two p-type polysilicon layers 33 and 35, another conductive layer 37, and another anti-fuse 39 ~~and the n-type polysilicon layer 25 of the first stack circuit~~. The conductive layer 37 of the second stack circuit 31 is located between the p-type polysilicon layers 33 and 35. The anti-fuse 39 is located between the p-type polysilicon layer 35 and the conductive layer 37. Hence, the second stack circuit 31 has a p-type polysilicon/conductive layer/anti-fuse/p-type polysilicon (P/C/A/P) setup. The second stack circuit 31 crosses over and is perpendicular to the first stack circuit 21 ~~vertically~~. In this invention, memory capacity of the three-dimensional structure depends on the number of stack circuits over the substrate. Hence, stacking more circuits on top of the substrate will increase the overall memory capacity.

Please amend paragraph [0023] of the specification as follow:

[0023] The p-type polysilicon layer 212, the conductive layer 214, the anti-fuse 216, ~~and~~ the p-type polysilicon layer 218 are patterned to form an array of linear second stack circuits ~~210~~ 220 each having ~~an n-type polysilicon/~~p-type polysilicon/conductive layer/anti-fuse/p-

type polysilicon (~~N~~P/C/A/P) composite layer setup. In the same patterning process, the n-type polysilicon layer 208 is also patterned to form the n-type polysilicon layer 208a, wherein the pattern of the n-type polysilicon layer 208a is substantially conformal to the shape of the interaction between each second stack circuit 220 and each first stack circuit 210. In essence, each first stack circuit 210 has the n-type polysilicon layer 202, the conductive layer 204, the anti-fuse 206 and the n-type polysilicon layer 208a composite layer setup. Further, ~~T~~the second stack circuits 220 are oriented in a direction perpendicular to and ~~vertically~~ above the first stack circuits 210. In patterning the second stack circuits 220, the anti-fuse serves as an etching stop layer. Thereafter, a dielectric layer 12 is formed in the space between the second stack circuits 220. The dielectric layer 12 is, for example, a silicon oxide layer, a silicon nitride layer or a spin-coated glass layer. The dielectric layer 12 is formed, for example, by performing a high-density plasma chemical vapor deposition or a spin-coating process.

Please amend paragraph [0027] of the specification as follow:

[0027] The n-type polysilicon layer 222, the conductive layer 224, the anti-fuse 226, the n-type polysilicon layer 228 and the p-type polysilicon layer 218 are patterned, wherein the patterned n-type polysilicon layer 222, the patterned conductive layer 224, the patterned anti-fuse 226, and the patterned n-type polysilicon layer 228 ~~to~~ form an array of linear third stack circuits 230 each having an ~~p-type polysilicon/~~n-type

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polysilicon/conductive layer/anti-fuse/n-type polysilicon (~~P~~N/C/A/N) composite layer setup. In the same patterning process, the p-type polysilicon layer 218 is also patterned to form the p-type polysilicon layer 218a, wherein the pattern of the p-type polysilicon layer is substantially conformal to the shape of the interaction between each third stack circuit 230 and each second stack circuit 220. In essence, each second stacked circuit 220 has the p-type polysilcion layer 212, the conductive layer 214, the anti-fuse 216 and the p-type polysilicon layer 218a composite layer setup. Further, the third stack circuits 230 are oriented in the same direction as the first stack circuits 210. Thereafter, a dielectric layer 18 is formed in the space between the ~~first~~ third stack circuits ~~210~~230 and the p-type polysilicon layer 281a, for example, by performing a high-density plasma chemical vapor deposition or a spin-coating process. The dielectric layer 18 is, for example, a silicon oxide layer, a silicon nitride layer or a spin-coated glass layer.

Please amend paragraph [0030] of the specification as follow:

[0030] The p-type polysilicon layer 232, the conductive layer 234, the anti-fuse 236, the p-type polysilicon layer 238 and the n-type polysilicon layer 228 are patterned, wherein the patterned p-type polysilicon layer 232, the patterned conductive layer 234, the patterned anti-fuse 236, and the patterned p-type polysilicon layer 238 ~~to~~ form an array of linear fourth stack circuits 240 each having a ~~n-type polysilicon/~~p-type polysilicon/conductive layer/anti-fuse/p-type polysilicon (~~N~~P/C/A/P) composite layer setup.

In the same patterning process, the n-type polysilicon layer 228 is also patterned to form the n-type polysilicion layer 228a, wherein the pattern of the n-type polysilicon layer 228a is substantially conformal to the shape of the interaction between each third stack circuit 230 and each fourth stack circuit 240+. In essence, each third stacked circuit 230 has the n-type polysilicon layer 222, the conductive layer 224, the anti-fuse 226, and the n-type polysilicon layer 228a composite layer setup. Further, the fourth stack circuits 240 are oriented in a direction identical to the second stack circuits 220. Thereafter, a dielectric layer 20 is formed in the space between the fourth stack circuits 240 above the anti-fuse 226. The dielectric layer 20 is, for example, a silicon oxide layer, a silicon nitride layer or a spin-coated glass layer. The dielectric layer 20 is formed, for example, by performing a high-density plasma chemical vapor deposition or a spin-coating process.

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